



矽杰微电子
XIJIE MICROELECTRONICS

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XC8P8600

8 OTP
Ver 1.4

矽杰
XIJIE MIC

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XIJIE MICROELECTRONICS

电子
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XC8P8600

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V1.0		
V1.1	TCC PWM	LVR
V1.2	ADCON	
V1.3	GPIO	
V1.4	ADC ADPS/ADCVS/CONT/STATUS	

CONT

Bit. 3(PAB)

Bit. 2 0(PSR2 PSR0)

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1.

1.1

CPU

2K× 14-Bi t OTP ROM	I HRC
64× 8-Bi t SRAM	8MHz/910KHz
7	I LRC
9	14KHz(5V)/8KHz(3V)
Di sabl e 1.2V 1.6V 1.8V 2.4V	2Cl ock 4Cl ock 8Cl ock 16Cl ock 32Cl ock
2.7V 3.3V 3.6V 3.9V	
1.2 mA 4MHz/5V	
5 μA 13KHz/5V	8Bi t /
1 μA	3 8Bi t
	5 12Bi t ADC

I/O

1 I0 P6	
6 I/O	TCC
P6	
6 I/O	
5 I/O	T1/PWM
6 I/O	ADC
P63()	
P60	

WDT
ADC
ADC

VLVR2.7V	5.5V Fcpu=0	8MHz
VLVR2.4V	5.5V Fcpu=0	4MHz
VLVR1.8V	5.5V Fcpu=0	2MHz

1K

XC8P8600-DI P8
XC8P8600-SOP8
XC8P8600-SOT23-6

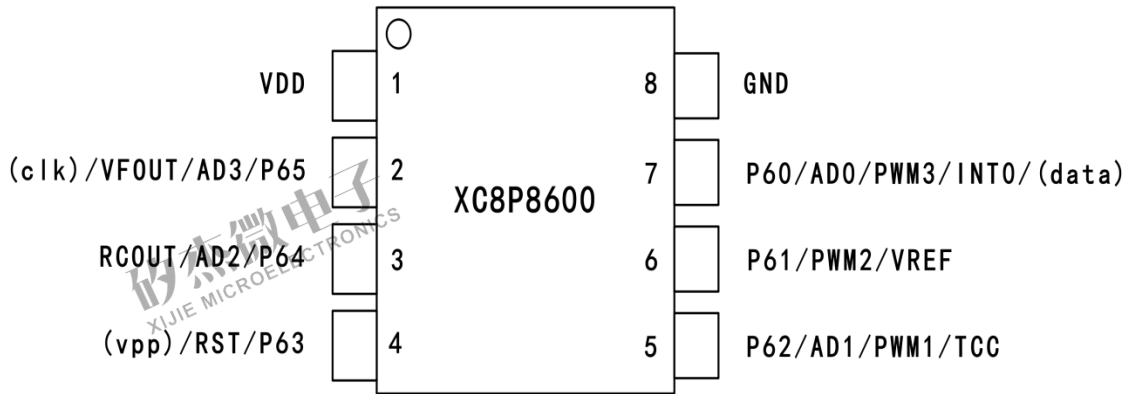
-40 -85



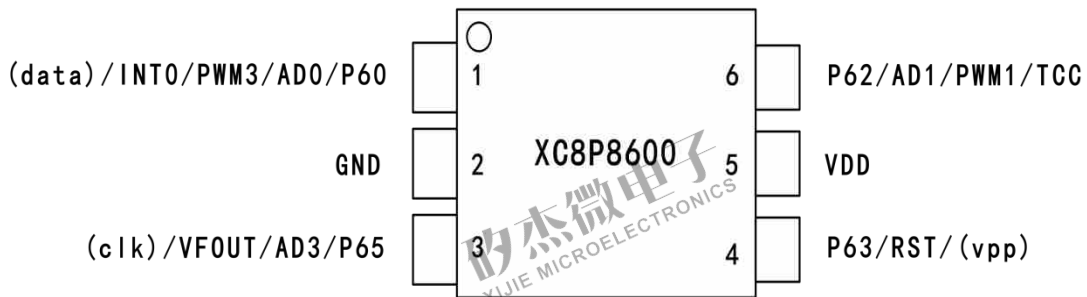
XC8P8600

1.2

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XC8P8600-8PIN



XC8P8600-6PIN

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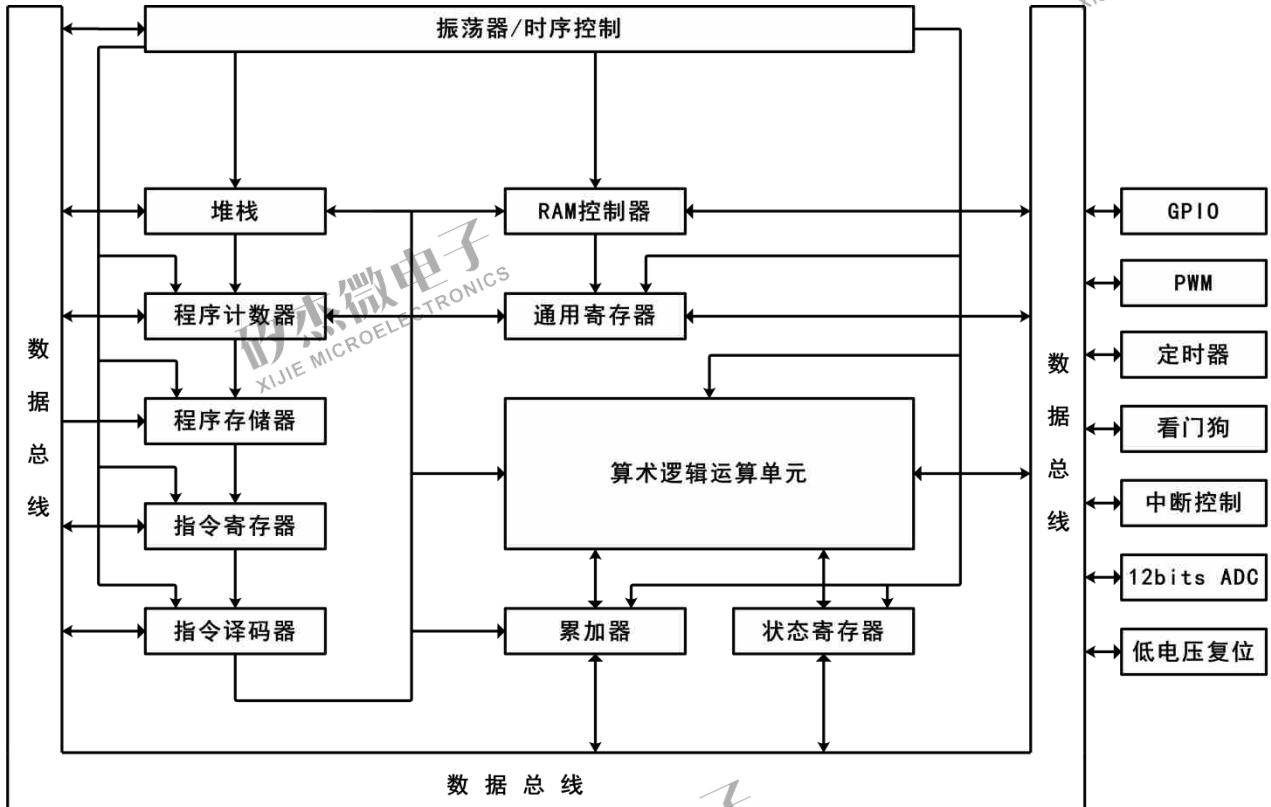


1.3

		I/O	
P60	P60	I/O	GPIO
	INT0	I	
	PWM3	O	PWM3
	AD0	I	ADC0
	data	I (SMT)	
P61	P61	I/O	GPIO
	PWM2	O	PWM2
	EXVREF	I	
P62	P62	I/O	GPIO
	TCC	I	TCC
	PWM1	O	PWM1
	AD1	I	ADC1
P63	P63	I/O	GPIO
	RST	I	
	vpp	I	
P64	P64	I/O	GPIO
	RCOUT	O	
	AD2	I	ADC2
P65	P65	I/O	GPIO
	VFOUT	O	ADC
	AD3	I	ADC3
	clk	I (SMT)	
	VDD	-	
	VSS	-	



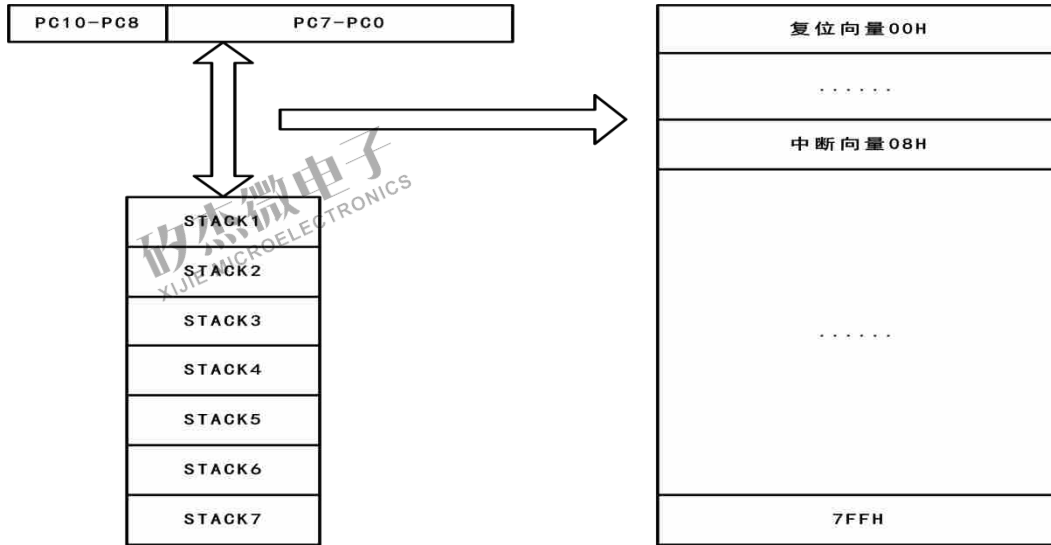
1.4





2.

2.1



2.2

R \ IOC IOC IR/IW

	R	IOIC
0x00	R0/IAR()	
0x01	R1/TCC()	CONT()
0x02	R2/PC()	
0x03	R3/STATUS()	
0x04	R4/RSR(RAM)	
0x05		
0x06	R6/PORT6(P6)	IOIC6/P6CR(P6)
0x07	R7/ADCON(ADC)	IOIC7/ADCVS AD
0x08	R8/PWMCON(PWM)	IOIC8/ADATH ADC 8
0x09	R9/PRD(PWM)	IOIC9/PHDCR()
0x0A	RA/PDC1(PWM1)	IOICA/ADPS ADC 4
0x0B	RB/PDC2(PWM2)	IOICB/PDCR()
0x0C	RC/PDC3(PWM3)	IOICC/ADATL AD 8
0x0D	RD/IC1 ECR()	IOICD/PHCR()
0x0E	RE/CPUCON(CPU)	IOICE/WDTCR(WDT)
0x0F	RF/ISR()	IOICF/IMR()
0x10		
...		
0x4F		



3.

3.1

3.1.1 RPAGE R0/IAR ()

00H(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
IAR	RI ND<7: 0>							
/	R							
	X							

R0

R4 RAM

7 FSR<6: 0>

3.1.2 RPAGE R1/TCC()

01H(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
TCC(R)	TCC<7>	TCC<6>	TCC<5>	TCC<4>	TCC<3>	TCC<2>	TCC<1>	TCC<0>
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

TCC 8Bi t

/

TCC

TCC INTO

1 CONT. 4

PAB CONT. 3

TCC TCC

0

3.1.3 RPAGE R2/PCL()

02H(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
PCL	PCL<7>	PCL<6>	PCL<5>	PCL<4>	PCL<3>	PCL<2>	PCL<1>	PCL<0>
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

PC

CPU

CPU

PC

1

XC8P8600

11

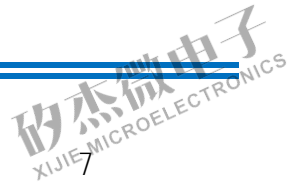
PC

PCL

PC<10: 8>



XC8P8600



XC8P8600

PC

PC

XC8P8600

7

- (1) PC 7 11 2K× 14Bi t ROM XC8P8600
- (2) PC PC
- (3) " JMP" 11 JMP 2K
JMP 11 PC +1
- (4) " RET" PC
- (5) PC 008
- (6) 7 8
1 9 2

3. 1. 4 RPAGE R3/STATUS()

03H(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
STATUS	RST	GB1	GB0	T	P	Z	DC	C
/	R	R/W	R/W	R	R	R/W	R/W	R/W
	0	0	0	1	1	X	X	X

Bi t<7> RST-

0

1

Bi t<6> GB1-

Bi t<5> GB0-

Bi t<4> T-

0 WDT

1 " SLEEP" " CWDT"

Bi t<3> P-

0 " SLEEP"

1 " CWDT"

Bi t<2> Z-

" 1"

0

0

1

0

Bi t<1> DC-





0 /
1 /
Bit<0> C-
0 /
1 /
T/P

	RST	T	P
	0	1	1
RESET	0		
RESET	0	1	0
WDT	0	0	
WDT	0	0	0
	1	1	0
CWDT		1	1
SLEEP		1	0

3.1.5 RPAGE R4/RSR(RAM)

04H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FSR	-	FSR<6>	FSR<5>	FSR<4>	FSR<3>	FSR<2>	FSR<1>	FSR<0>
/	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	1	X	X	X	X	X	X	X

FSR<6:0>

RAM

0X00 0X4F

FSR

R0

FSR

R0

FSR

3.1.6 RPAGE R6/PORT6(P6)

06H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORT6	-	-	P65	P64	P63	P62	P61	P60
/	R	R	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	1	1	1	1	1	1

P6

8



3.1.7 RPAGE R7/ADCON(ADC)

07H(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
ADCON	ADRUN	ADPD	VREFS	CALI	SIGN	VOF<2>	VOF<1>	VOF<0>
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

Bi t<7> ADRUN

1 ADC

0 ADC

Bi t<6> ADPD

1 ADC

0 ADC

ADC

Bi t<5> VREFS

1 ADC

P61

0 ADC

Bi t<4> CALI

1 ADC 0

0 ADC 0

Bi t<3> SIGN

1 ADC 0

0 ADC 0

Bi t<2:0> VOF<2:0> ADC 0

VOF<2>	VOF<1>	VOF<0>	
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB



3.1.8 RPAGE R8/PWMCON(PWM)

08H(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
T1	T1EN	PWM3EN	PWM2EN	PWM1EN	T1PTEN	T1PSR<2>	T1PSR<1>	T1PSR<0>
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

Bi t<7> T1EN -T1/PWM

1

0

PRD T1 PRD T1 1

Bi t<6: 4> PWM3EN PWM1EN - PWM3 PWM1

1

PWM3(P60), PWM2(P61), PWM1(P62)

0

Bi t<3> T1PTEN -T1

Bi t<2:0> T1PSR2 T1PSR1

T1PTEN	T1PSR<2>	T1PSR<1>	T1PSR<0>	
0	0	0	0	1: 1
1	0	0	0	1: 2
1	0	0	1	1: 4
1	0	1	0	1: 8
1	0	1	1	1: 16
1	1	0	0	1: 32
1	1	0	1	1: 64
1	1	1	0	1: 128
1	1	1	1	1: 256

3.1.9 RPAGE R9/PRD(PWM)

09H(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
PRD	PRD<7>	PRD<6>	PRD<5>	PRD<4>	PRD<3>	PRD<2>	PRD<1>	PRD<0>
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

Bi t<7:0> PRD<7:0>-PWM



3. 1. 10 RPAGE RA/PDC1(PWM1)

OAH(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
PDC1	PDC1<7>	PDC1<6>	PDC1<5>	PDC1<4>	PDC1<3>	PDC1<2>	PDC1<1>	PDC1<0>
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

Bi t<7:0> PDC1<7:0>-PWM1

3. 1. 11 RPAGE RB/PDC2(PWM2)

OBH(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
PDC2	PDC2<7>	PDC2<6>	PDC2<5>	PDC2<4>	PDC2<3>	PDC2<2>	PDC2<1>	PDC2<0>
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

Bi t<7:0> PDC2<7:0>-PWM2

3. 1. 12 RPAGE RC/PDC3(PWM3)

OCH(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
PDC3	PDC3<7>	PDC3<6>	PDC3<5>	PDC3<4>	PDC3<3>	PDC3<2>	PDC3<1>	PDC3<0>
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

Bi t<7:0> PDC3<7:0>-PWM3

3. 1. 13 RPAGE RD/ICIECR()

ODH(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
ICIECR	-	-	IEN<5>	IEN<4>	IEN<3>	IEN<2>	IEN<1>	IEN<0>
/	R	R	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

Bi t<5:0> IEN<5:0>-P6

1

0

OPTION

P6

0x0D



3. 1. 14 RPAGE RE/CPUCON(CPU)

OEH(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
CPUCON	IPWM1	PWMCKS	TCCCKS	PWMWE	TCCWE	STPHX	CLKMD	IDLE
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

Bi t<7> IPWM1

1 PWM1

0 PWM1

Bi t<6> PWMCKS

1

0

Bi t<5> TCCCKS

1

0

Bi t<4> PWMWE

1 PWM

0 PWM

Bi t<3> TCCWE

1 TCC

0 TCC

Bi t<2> STPHX

1

0

Bi t<1> CLKMD

1

RC

0

IRC

CLKMD=1

STPHX=1

STPHX=0

CLKMD=0

Bi t<0> IDLE

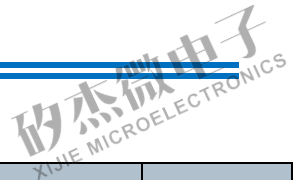
1

SLEEP

TCC PWM

0

SLEEP



3. 1. 15 RPAGE RF/ISR()

OFH(R)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
ISR	-	-	-	ADIF	T1IF	EXIF	ICIF	TCIF
/	R	R	R	R	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

Bi t<7: 5>

Bi t<4> ADIF - ADC

Bi t<3> T1IF -T1/PWM

Bi t<2> EXIF-

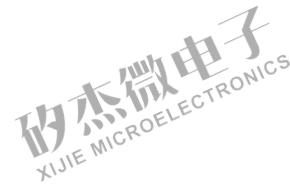
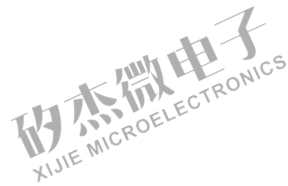
Bi t<1> ICIF-P6

Bi t<0> TCIF-TCC

1	0
0	

MOV RF, A

BTC AND RF, A





3. 2

3. 2. 1 CONT(

01H(I0C)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
CONT	-	INT	TS	TE	PAB	PSR2	PSR1	PSR0
/	R	R	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	1	1	1	1

Bi t<7>

Bi t<6> INT-

0

1

Bi t<5> TS-TCC

0

1

P62

Bi t<4> TE-TCC

0 TCC

1 TCC

Bi t<3> PAB-

0

TCC

1

WDT

Bi t<2:0> PSR2 PSR0-TCC/WDT

PSR2	PSR1	PSR0	TCC	WDT
0	0	0	1: 2	1: 1
0	0	1	1: 4	1: 2
0	1	0	1: 8	1: 4
0	1	1	1: 16	1: 8
1	0	0	1: 32	1: 16
1	0	1	1: 64	1: 32
1	1	0	1: 128	1: 64
1	1	1	1: 256	1: 128

PAB PSR2 PSR0

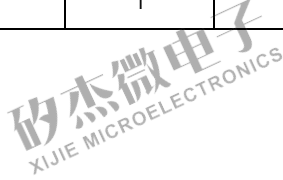


3.2.2 IOPAGE I0C6/P6CR(P6)

06H(I0C)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
P6CR	-	-	P6CR<5>	P6CR<4>	P6CR<3>	P6CR<2>	P6CR<1>	P6CR<0>
/	R	R	R/W	R/W	R/W	R/W	R/W	R/W
	1	1	1	1	1	1	1	1

Port6

1
0



3.2.3 IOPAGE I0C7/ADCVS(AD)

07H(I0C)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
ADCVS	ADCKS<1>	ADCKS<0>	ADICS<2>	ADICS<1>	ADICS<0>	VREF<2>	VREF<1>	VREF<0>
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	1	1	1	1	1	1	1	1

Bi t<7:6> ADCKS<1:0>

CLKMD	ADCKS<1>	ADCKS<0>	ADC
0	0	0	Fosc/16
0	0	1	Fosc/4
0	1	0	Fosc/64
0	1	1	Fosc/1
1	X	X	Fosc/1

Bi t<5:3 > ADICS<2:0>

ADICS<2>	ADICS<1>	ADICS<0>	ADC
0	0	0	AD0 P60
0	0	1	AD1 P62
0	1	0	AD2 P64
0	1	1	AD3 P65
1	0	0	AD4

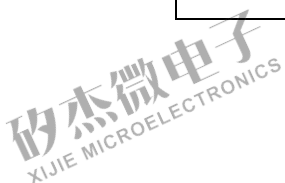
AD4

VREFS=0

VREFS=1

Bi t<2:0> VREF<2:0>

VREF<2>	VREF<1>	VREF<0>	
0	0	0	VDD
0	0	1	4V
0	1	0	3V
0	1	1	2V
1	0	0	1.5V





3.2.4 IOPAGE IOC8/ADATH(AD 8)

08H(IOC)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
ADATH	ADTA<11>	ADTA<10>	ADTA<9>	ADTA<8>	ADTA<7>	ADTA<6>	ADTA<5>	ADTA<4>
/	R	R	R	R	R	R	R	R
	X	X	X	X	X	X	X	X

3.2.5 IOPAGE IOC9/PHDCR()

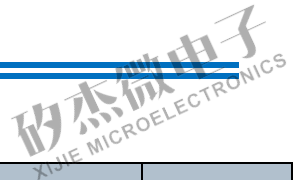
09H(IOC)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
PHDCR	-	-	P6PD<5>	P6PD<4>	-	-	-	-
/	R	R	R/W	R/W	R	R	R	R
	1	1	1	1	1	1	1	1

Bi t<5: 4> P6<5: 4>
 0
 1

3.2.6 IOPAGE IOCA/ADPS(AD 4)

0AH(IOC)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
ADPS	ADEN<3>	ADEN<2>	ADEN<1>	ADEN<0>	ADAT<11>	ADAT<10>	ADAT<9>	ADAT<8>
/	R/W	R/W	R/W	R/W	R	R	R	R
	1	1	1	1	X	X	X	X

Bi t<7: 4> ADEN<3 0>--AD
 0 AD<3 0> (P65/P64/P62/P60) GPI 0
 1 AD<3 0> (P65/P64/P62/P60)
 Bi t<3: 0> ADAT<11: 8>--AD



3.2.7 IOPAGE IOCB/PDCR()

OBH(IOC)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
PDCR	-	P6PD<2>	P6PD<1>	P6PD<0>	-	-	-	-
/	R	R/W	R/W	R/W	R	R	R	R
	1	1	1	1	1	1	1	1

Bi t7

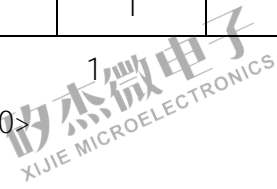
Bi t<6: 4> P6<2: 0>

0

1

Bi t<3: 0>

1

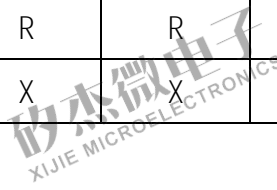


3.2.8 IOPAGE IOCC/ADATL(AD 8)

OCH(IOC)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
ADATL	ADTA<7>	ADTA<6>	ADTA<5>	ADTA<4>	ADTA<3>	ADTA<2>	ADTA<1>	ADTA<0>
/	R	R	R	R	R	R	R	R
	X	X	X	X	X	X	X	X

AD

8



3.2.9 IOPAGE IOCD/PHCR()

ODH(IOC)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
PHCR	-	-	P6PH<5>	P6PH<4>	P6PH<3>	P6PH<2>	P6PH<1>	P6PH<0>
/	R	R	R/W	R/W	R/W	R/W	R/W	R/W
	1	1	1	1	1	1	1	1

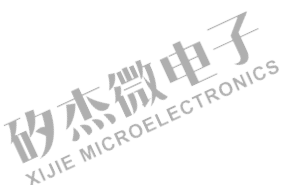
Port6

0

1

OPTION

P63





3.2.10 IOPAGE IOCE/WDTCR(WDT)

OEH(IOC)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
WDTCR	WDTEN	EIS	ADWE	VFOE	-	-	-	-
/	R/W	R/W	R/W	R/W	R	R	R	R
	1	0	0	0	1	1	1	1

Bi t<7> WDTEN-WDT
1
0



WDTEN OPTION

Bi t<6> EIS-P60
1 P60 I/O P6CR Bi t0 " 1"
0 P6 P60 I/O INTO

Bi t<5> ADWE-AD
1 ADC
0 ADC

Bi t<4> VFOE-
1 P65 VREF<2 0>
0 P65 I0

Bi t<3:0>



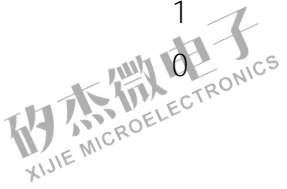
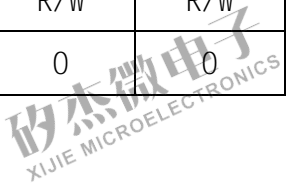
3.2.11 IOPAGF IOCF/IMR()

OFH(IOC)	Bi t7	Bi t6	Bi t5	Bi t4	Bi t3	Bi t2	Bi t1	Bi t0
IMR	-	-	-	ADIE	T1IE	EXIE	ICIE	TCIE
/	R	R	R	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

Bi t<7:5>

Bi t<4> ADIE-AD
1
0

Bi t<3> T1IE-T1
1
0





XC8P8600

Bit<2> EXIE-

1 P60

0

Bit<1> P6ICIE-P6

1

0

Bit<0> TCIE-TCC

1

0

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XIJIE MIC

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电子
ELECTRONICS

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3.3

XC8P8600

5

“ EI ”

008H

		EI + EXIE=1	EXIF
		EI + ICIE=1	ICIF
	TCC	EI + TCIE=1	TCIF
	PWM	EI + T1IE=1	T1IF
	ADC	EI + ADIE=1	ADIF

RPAGE RF

IOCF

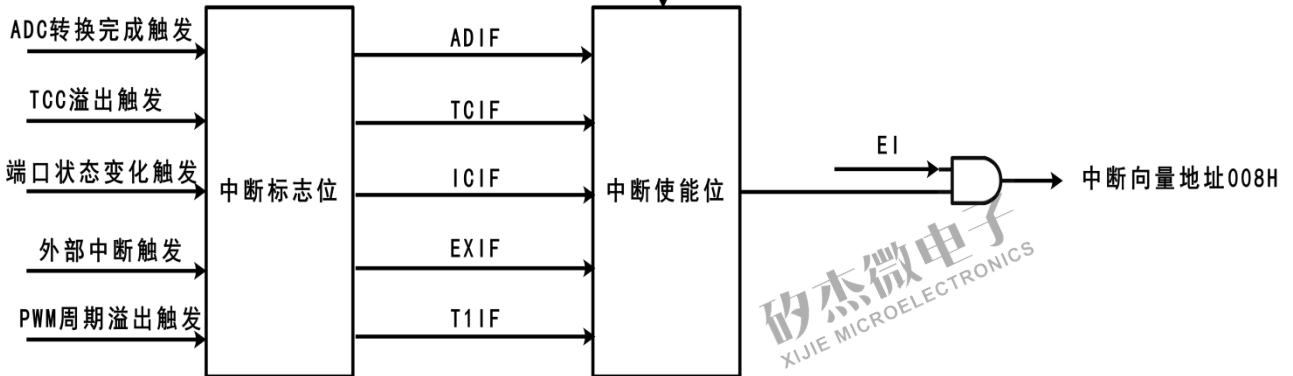
“ EI ”

“ DI ”

008H

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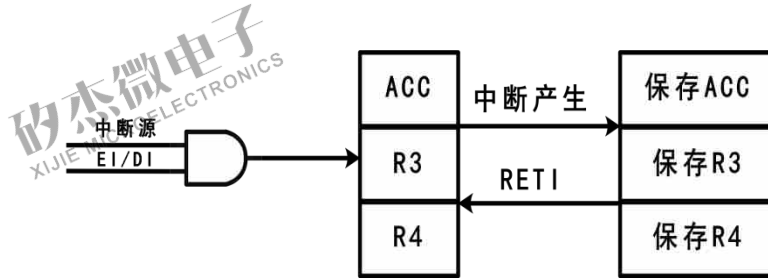


3.3.1

ACC R3 R4

ACC R3 R4

ACC R3 R4





3.4

3.4.1

XC8P8600

4

POR

RESET

WDT

LVR

PC

0000H

MCU

VDD

RC

3.4.2 WDT

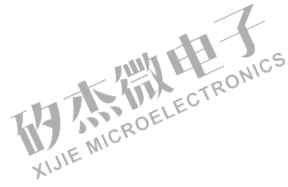
I/O

RAM



3.4.3 POR

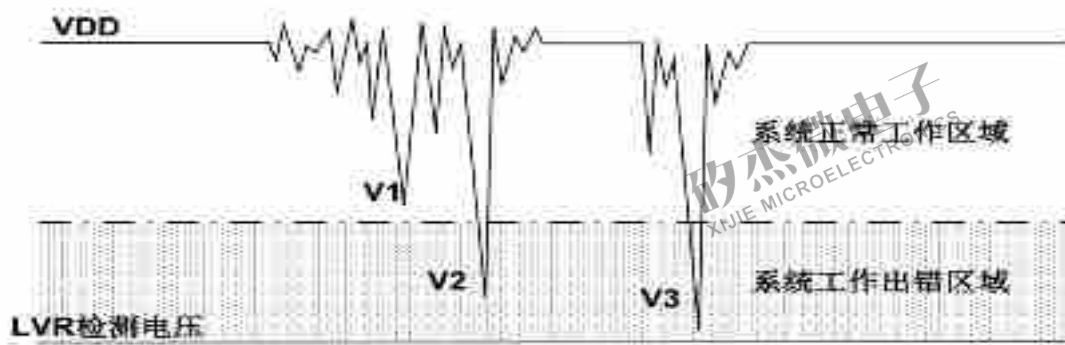
LVR



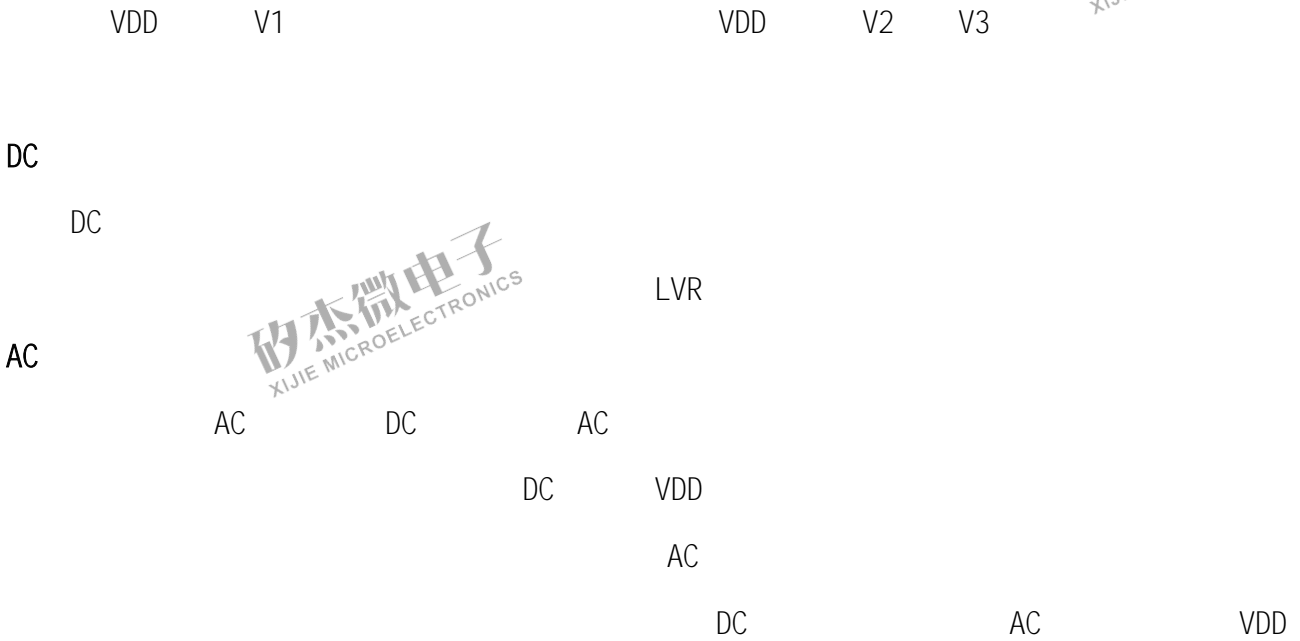
OPTION

PWRT	WDT	
PWRT=WDT		4.5ms()
PWRT=WDT		18ms()
PWRT=WDT		72ms()
PWRT=WDT		288ms()
PWRT	WDT	140us()

3.4.4 LVR

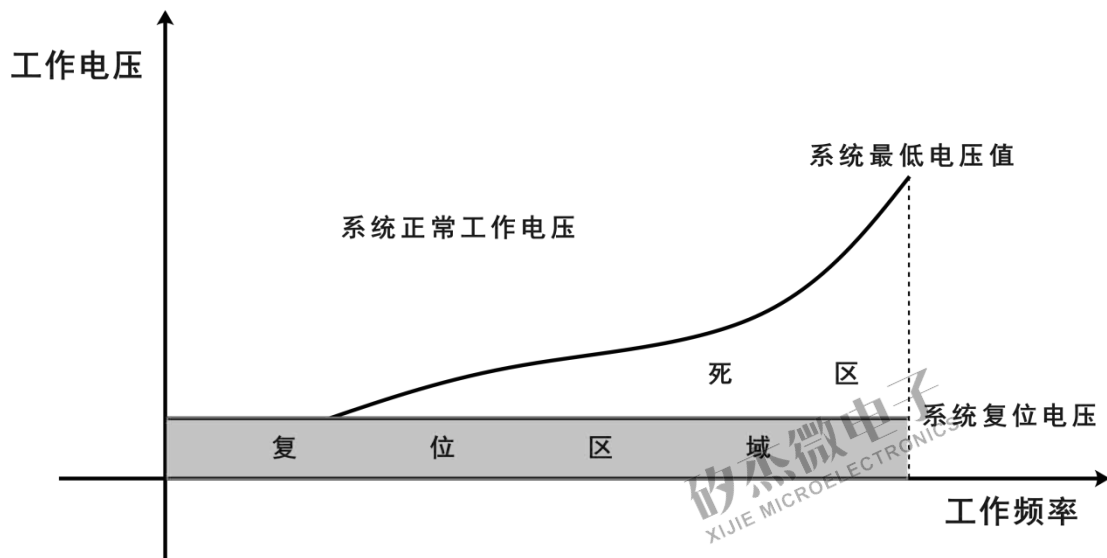
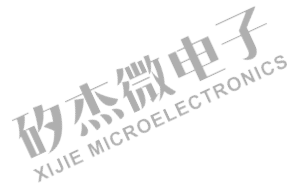


VDD



3.4.5

LVR



LVR





XC8P8600

LVR

IRC		Clocks	LVR
IRC-8MHz		2 Cl ocks	LVR=2. 7V
IRC-8MHz		2 Cl ocks	LVR=2. 4V
IRC-910KHz		2 Cl ocks	LVR=1. 8V
IRC-910KHz		2 Cl ocks	LVR=1. 8V

1

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= IRC

+ Cl ocks

2

LVR

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3.5

XC8P8600

4

I RC

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TCC PWM ADC

WDT

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XIJIE MIC

I HRC		STPHX	STPHX	
I LRC				
CPU				
TCC				
PWM				
ADC				
			TCC, PWM, ADC	
	-	-	P6I C, TCC, PWM, ADC WDT, RESET	P6I C, WDT, RESET
	WDT	WDT	WDT	WDT

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3.5.1

RC

CPU



3.5.2

CPU

CLKMD

CLKMD=0

RC

CLKMD=1

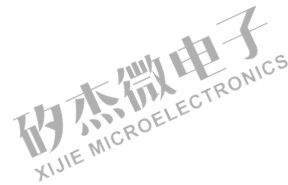
SPTHX



RC

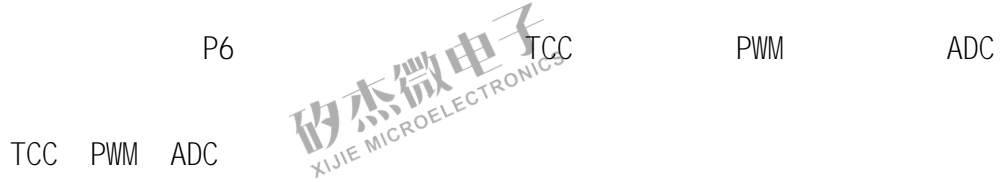
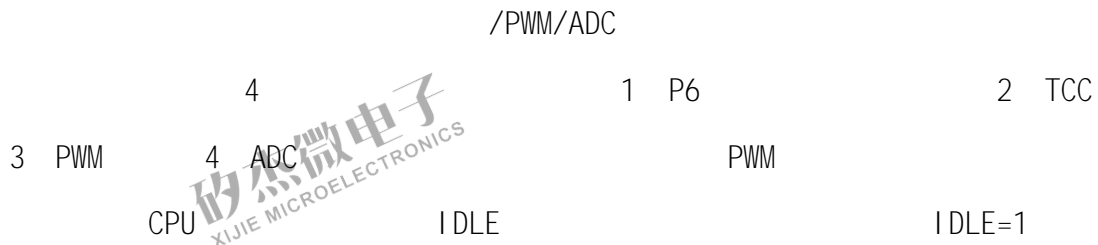
SPTHX=1

CPU

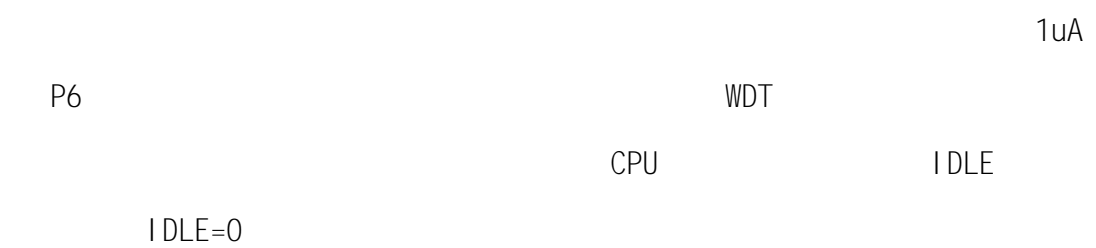




3.5.3



3.5.4



1uA

P6

WDT



3.6

XC8P8600 IRC OPTION

IRC	RC	RCM	910K/8M

3.6.1 RC

XC8P8600 RC 8MHz

RC 8MHz 910KHz OPTION

IRC

Fi rc	IRC
8 M	IRC 8MHz
910K	IRC 910KHz

XC8P8600

OPTION :

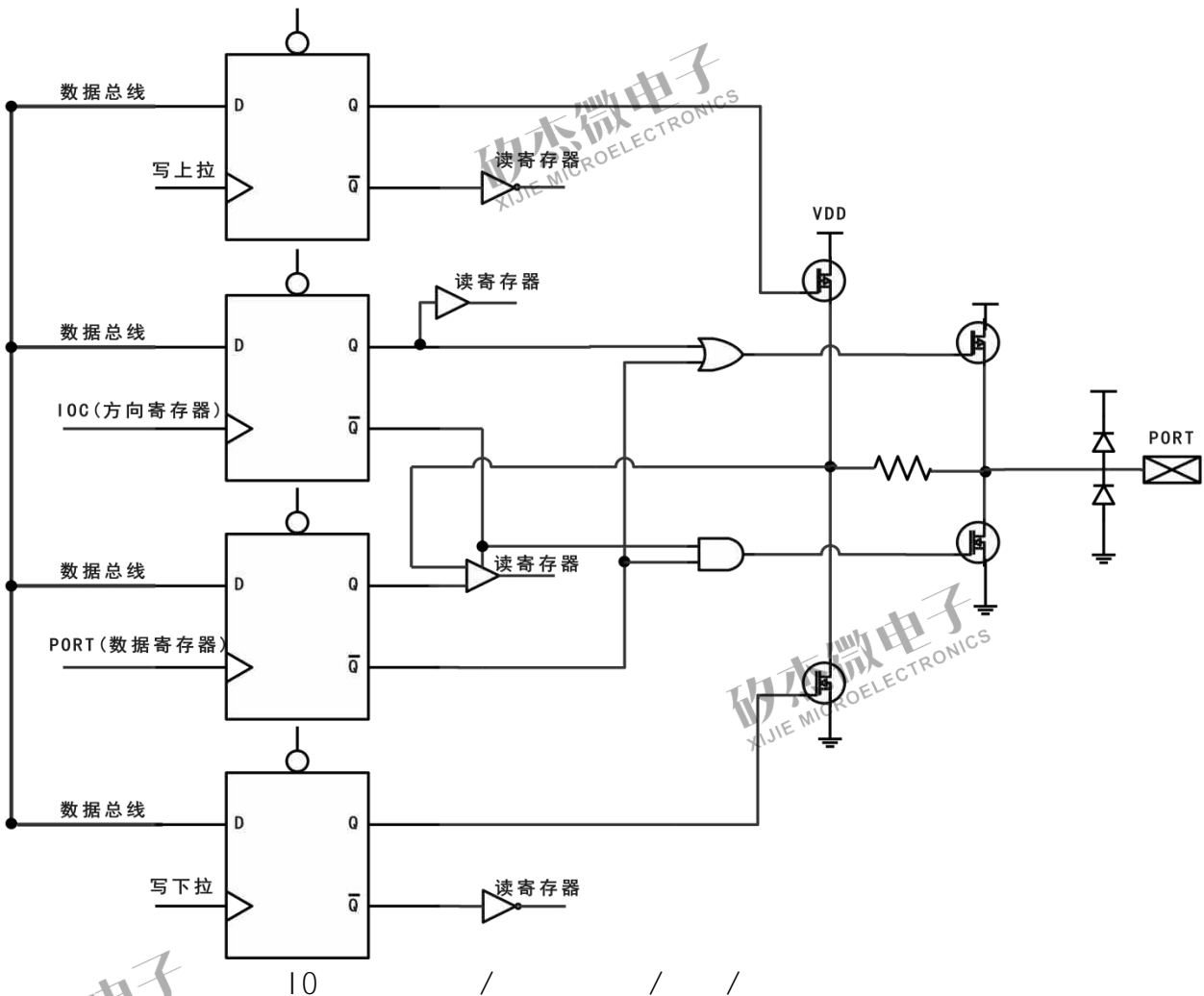
Clocks	Clocks
2cl ock	2cl ock
4cl ock	4cl ock
8cl ock	8cl ock
16cl ock	16cl ock
32cl ock	32cl ock



3.7 I/O

XC8P8600	1	I/O	6	6	I/O		
6		I/O	P60	P65			
5		I/O	P60	P62	P64	P65	
6	option		I/O	P60	P65	option	
3	option			P60	P61	P62	option
6			I/O	P60	P65		

3.7.1 GPIO





3.7.2

XC8P8600	6	I/O	P60	P65	" SLEEP"
				WDT	0
				SLEEP	DI

SLEEP	EI
-------	----

1	PORT6
---	-------

2	
---	--

3	PORT
---	------

4	
---	--

5	DI
---	----

6	" SLEEP"
---	----------

SLEEP

7	SLEEP
---	-------

1	PORT6
---	-------

2	
---	--

3	
---	--

4	PORT
---	------

5	" EI"
---	-------

6	" SLEEP"
---	----------

SLEEP

7	SLEEP
---	-------



3.7.3

XC8P8600

option

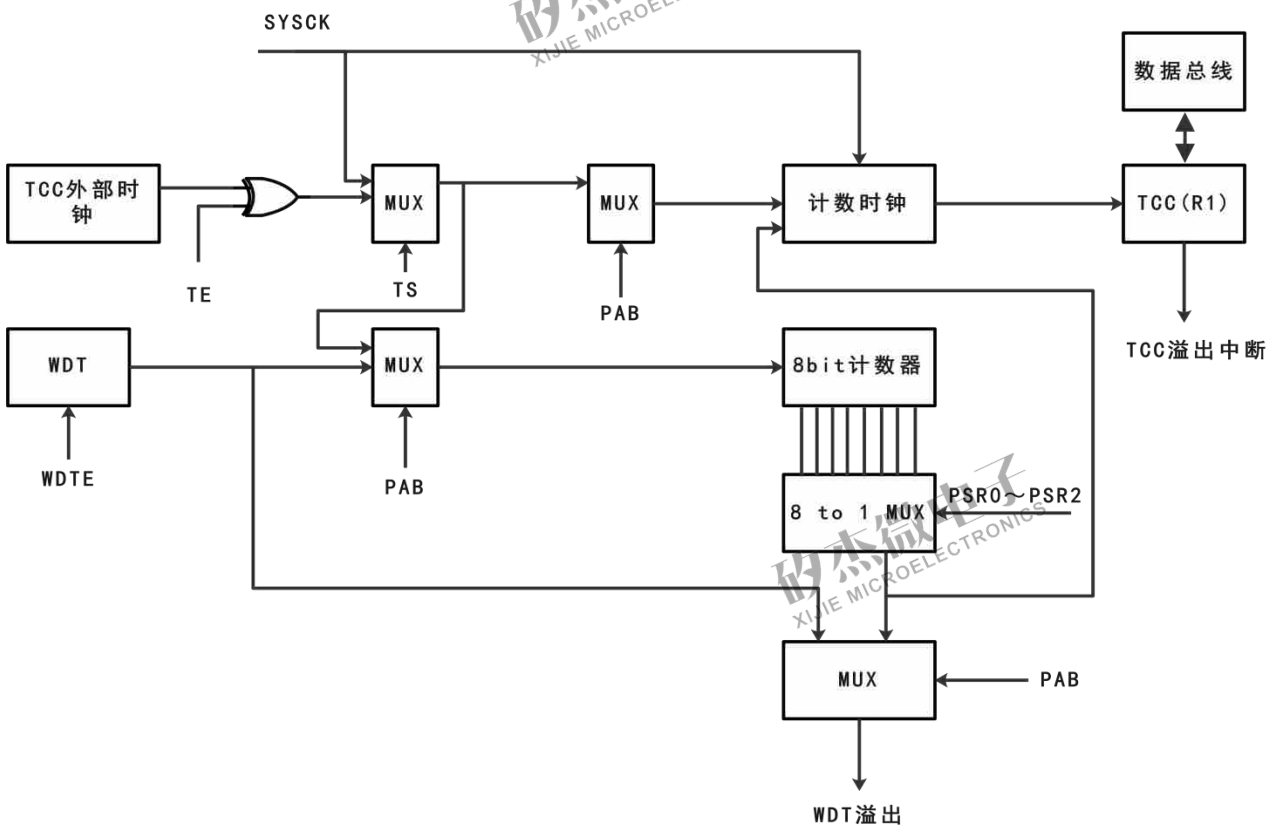
4

	SMT	HSMT	EMC	INV
P6.3	$0.56 \times VDD$	$0.2 \times VDD / 0.77 \times VDD$	$0.2 \times VDD / 0.32 \times VDD$	$0.54 \times VDD$
P6.0 P6.2	$0.25 \times VDD / 0.51 \times VDD$	$0.2 \times VDD / 0.77 \times VDD$	$0.2 \times VDD / 0.32 \times VDD$	$0.54 \times VDD$
P6.4 P6.5	$0.25 \times VDD / 0.51 \times VDD$	$0.2 \times VDD / 0.77 \times VDD$	$0.35 \times VDD$	$0.54 \times VDD$



3.8 TCC

XC8P8600	8	TCC	WDT
TCC	WDT	CONT	PAB
	TCC	TCC	PSR0 PSR2
WDT	" CWDT" " SLEEP"	WDT	
TCC (R1)	TCC 8Bit	WDT	
		TCC	
	Fm/Fs		
1	8Bit	TCC	CONT TCC
TCC			
IDLE	TCC		



TCC/WDT



3.8.1 TCC

TCC

CONT

CONT

TCC

1

IOCF

TCIE Bit0

1

EI

ACC STATUS R4

RETI

TCC



3.8.2 TCC

TCC

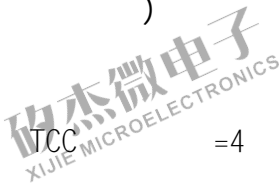
TCC

TCC

()

=2clock

Fosc=8 MHz



=4

TCC

=156

TCC

()

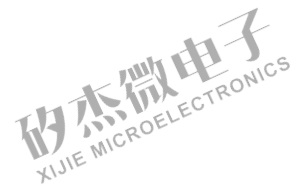
=1 MHz

TCC

=4

TCC

=156





3.9 PWM

XC8P8600

3

8 bit PWM

PWM

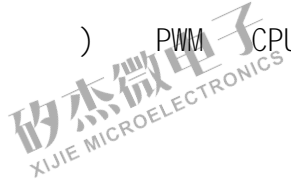
PWM

IDLE()

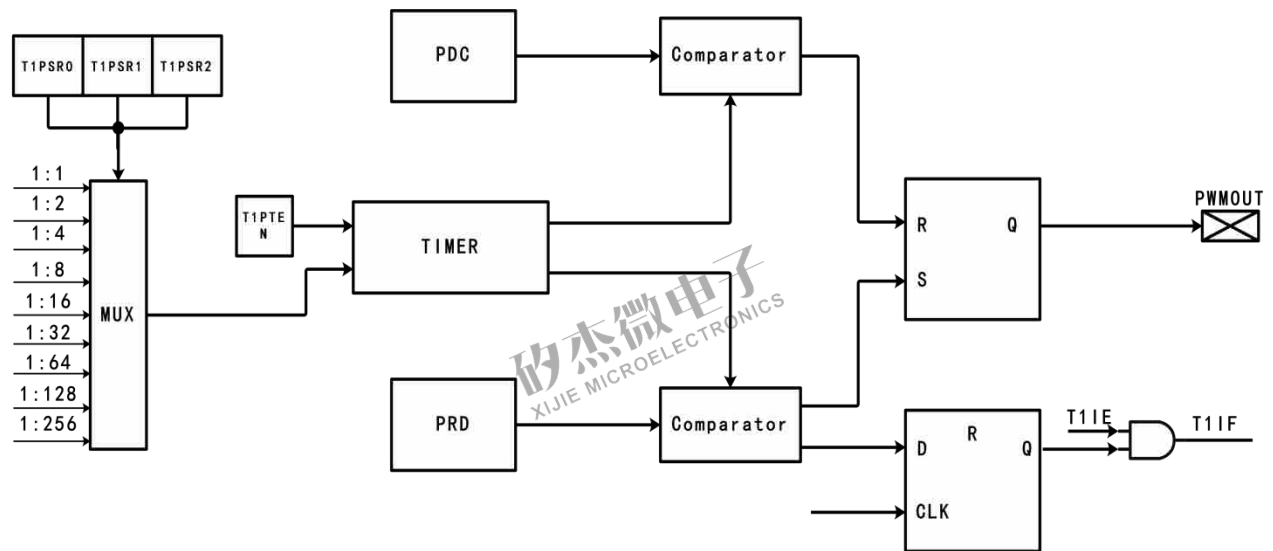
PWM CPU

PWMCKS=1

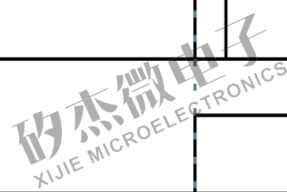
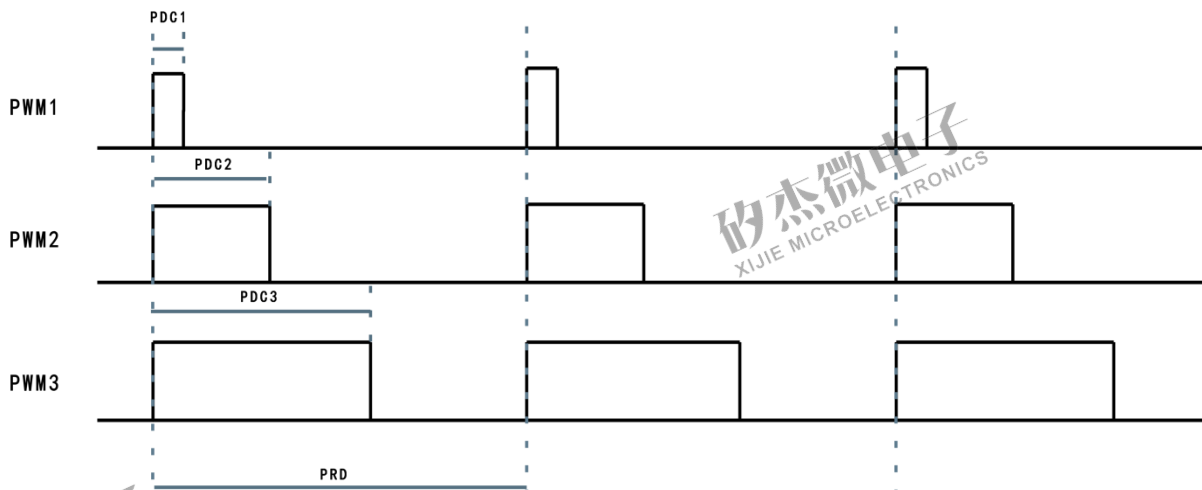
PWMWE



3.9.1 PWM



PWM



3

PWM





3.9.2 PWM

PWM 8bit T1 PWM
 PWM T1EN T1 T1PTEN T1PSR<2:0>
 T1

PWM PWM PRD T1 PRD

T1

PWM

PWM

PWM PDC1/PDC2/PDC3 PDC/T1

PWM

PRD=100 Fosc=8 MHz T1

=2

(-)

PWM

PWM

PDC1, PDC2, PDC3

T1

PDC1/PDC2/PDC3

PDC/T1

PDC/T1

T1

PWM

PDC1, PDC2, PDC3

PDC/T1

PWM

PDC=50 Fosc=8 MHz T1

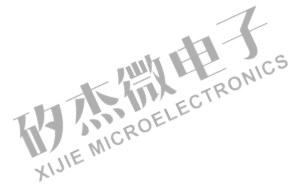
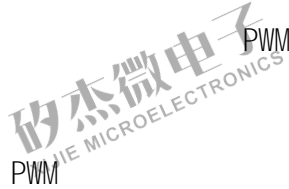
=2

(-)



3.9.3 PWM

PWMCON	PWM
PWM	
RPAGE-R9	PWM
PDCx	PWM
PWM	, " EI " " DI "

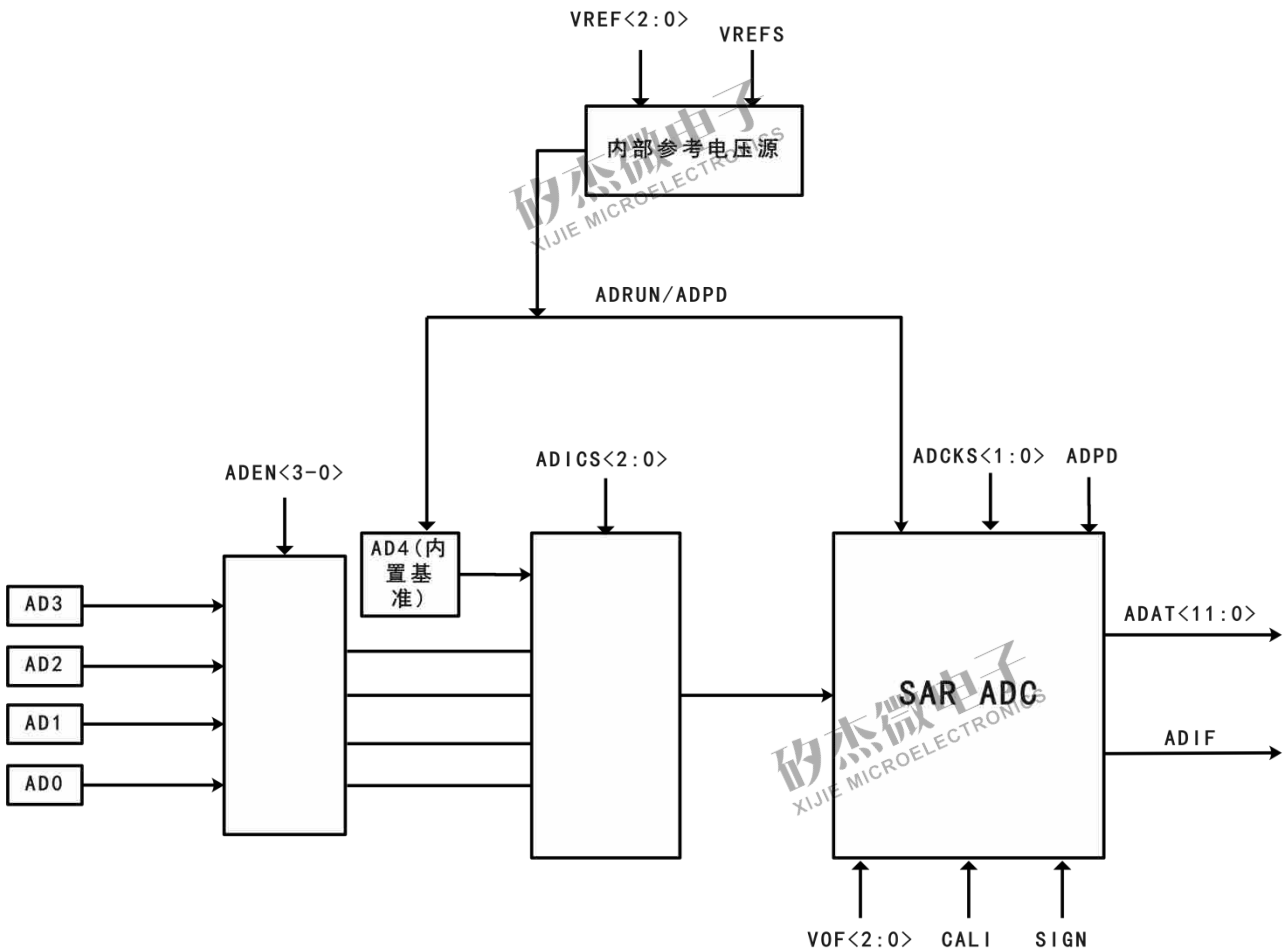




3.10 ADC

XC8P8600	ADC	SAR	4	4096		
		12	ADICS[2:0]			
AIN	SAR ADC	ADC	12	ADCKS[1:0]		
ADC	ADC	ADC				
	Vdd	4V	3V	2V	1.5V	ADCON
VREFS		ADC	ADPS			
	GPI O	ADC				
ADPD	ADRUN	ADC	ADC	ADIF	1	
ADATH	ADATL	ADPS	ADIE=1	ADC	AD	ADIF=1

ORG 0008H



ADC



3. 10. 1 ADC

ADC	P6	ADC	I0
ADPS	4	ADEN 0 3	I0
I0		ADC	ADCVS
ADICS[2:0]	ADICS[2:0]=000	AD0	ADICS[2:0]=001
P6	ADC	ADICS[2:0]	ADC
ADRUN	1	ADC	
VREFS = 1	P6.1	ADC	P6.1

3. 10. 2 ADC

ADC	6	ADCON	ADCVS	1	5
VDD	4V 3V 2V 1.5V	VREFS = 1	ADC		
P6.1		ADC		1V	VREFS = 0
ADC	VREF[2:0]	VHS[2:0] = 000	ADC		
VDD	VHS[2:0] = 001	ADC	4V	VHS[2:0] = 010	ADC
3V	VHS[2:0] = 011	ADC	2V	VHS[2:0] = 100	ADC
ADC	WDTCR	VFOE	1	P6.5	
		VDD		VDD	

3. 10. 3 ADC

ADCVS	ADICS<2:0>=100	AD4	ADC
VDD		ADC	
VREF<2:0>=100	1.5V	AD4	
1.5V	VDD	ADC	VDD



3. 10. 4 ADC

1	IOPAGE	IOCA/ADPS	ADEN3: ADEN0	
2	IOPAGE	IOC7/ADCVS	AD	ADC
	ADC	" ADPD=1"	AD	
3			ADIE=1	" EI "
4		AD		ADWE=1
5	" ADRUN=1"	AD		
6		IDLE/SLEEP		
7	ADRUN	0	AD	ADIF " 0"
8			AD	4



3. 11

TCC	IDLE
CPUCON	IDLE=1 , TCCWE=1 , TCCCKS=1
TCIE=1	
SLEEP	
TCC	IDLE
CPUCON	IDLE=1 , TCCWE=1 , TCCCKS=1 CLKMD=1 STPHX=1
TCIE=1	
SLEEP	
T1	IDLE
PWMCON	T1EN=1
PRD	
CPUCON	IDLE=1 , PWMWE=1 , PWMCKS=1
T1IE=1	
SLEEP	
T1	IDLE
PWMCON	T1EN=1
PRD	
CPUCON	IDLE=1 , PWMWE=1 , PWMCKS=1 CLKMD=1 STPHX=1
T1IE=1	
SLEEP	



4. OPTION

CODE OPTION			
			WDT
			WDT
Clocks	2 Clocks		2 Clocks
	4 Clocks		4 Clocks
	8 Clocks		8 Clocks
	16 Clocks		16 Clocks
	32 Clocks		32 Clocks
IRC	8M	IRC	8M
	910KHz	IRC	910KHz
			IRC
			IRC
	LVR=1.2V		1.2V
	LVR=1.6V		1.6V
	LVR=1.8V		1.8V
	LVR=2.4V		2.4V
	LVR=2.7V		2.7V
	LVR=3.3V		3.3V
	LVR=3.6V		3.6V
	LVR=3.9V		3.9V
OTP	2K	OTP	2K
	1K	OTP	1K
	1K	OTP	1K
2K/ 1K/ 1K	2K/ 1K/ 1K		
	2K/ 1K/ 1K		
			P63
			P63
P63	GPI0	P63	I/O
	GPI	P63	
	RST	P63	



XC8P8600

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	PWRT=WDT=4.5ms	=WDT	= 4.5ms
	PWRT=WDT=18ms	=WDT	= 18ms
	PWRT=WDT=72ms	=WDT	= 72ms
	PWRT=WDT=288ms	=WDT	= 288ms
	PWRT=140us, WDT=4.5ms	=140us, WDT	=4.5ms
	PWRT=140us, WDT=18ms	=140us, WDT	=18ms
	PWRT=140us, WDT=72ms	=140us, WDT	=72ms
	PWRT=140us, WDT=288ms	=140us, WDT	=288ms
	EMC	EMC	3.7.3
	SMT	SMT	3.7.3
	HSMT	HSMT	3.7.3
	INV	INV	3.7.3
P6		P6	0x0d
		P6	
		P60, P61, P62	
		P60, P61, P62	
ADC	2TAD	ADC	2TAD
	4TAD	ADC	4TAD
	8TAD	ADC	8TAD
	12TAD	ADC	12TAD
ADC		ADC	14
14		ADC	14
IRC	IRC LDO	IRC	LDO
	IRC VDD	IRC	VDD

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5.

ADD A, R	A+R A	Z, C, DC
ADD R, A	A+R R	Z, C, DC
AND A, R	A&R A	Z
AND R, A	A&R R	Z
CLRA	0 A	Z
CLR R	0 R	Z
INVA R	/R A	Z
INV R	/R R	Z
DA	A BCD	C
DECA R	R-1 A	Z
DEC R	R-1 R	Z
DJA R	R-1 A, skip if zero	-
DJ R	R-1 R, skip if zero	-
INCA R	R+1 A	Z
INC R	R+1 R	Z
IJA R	R+1 A, skip if zero	-
IJ R	R+1 R, skip if zero	-
MOV R, A	A R	-
MOV A, R	R A	Z
MOV R, R	R R	Z
OR A, R	A VR A	Z
OR R, A	A VR R	Z
SUB A, R	R-A A	Z, C, DC
SUB R, A	R-A R	Z, C, DC
XOR A, R	A R A	Z
XOR R, A	A R R	Z
IR R	IOCR A	-
IW R	A IOCR	-
CTR	CONT A	-
CTW	A CONT	-
BTC R, b	0 R(b)	-



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BTS R, b	1 R(b)	-
JBTC R, b	if R(b)=0, skip	-
JBTS R, b	if R(b)=1, skip	-
LCR R	R(n) R(n+1), R(7) C, C R(0)	C
LCA R	R(n) A(n+1), R(7) C, C A(0)	C
RCR R	R(n) R(n-1), R(0) C, C R(7)	C
RCA R	R(n) A(n-1), R(0) C, C A(7)	C
SWAP R	R(0-3) ↔ R(4-7)	-
SWAPA R	R(0-3) A(4-7), R(4-7) A(0-3)	-
ADD A, k	A+k A	Z, C, DC
AND A, k	A&k A	Z
MOV A, k	k A	-
OR A, k	A k A	Z
SUB A, k	k-A A	Z, C, DC
XOR A, k	A k A	Z
CALL k	PC+1 [SP], (Page, k) PC	-
DI		-
EI		-
JMP k	K (Page, k) PC	-
NOP		-
RET	[] PC	-
RETI	[] PC,	-
RETL k	k A, [] PC	-
SLEEP	0 WDT,	T, P
CWDT	0 WDT	T, P

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6.

6.1

.....	-40	85
.....	-65	150
.....	Vss-0.3V	Vdd+0.5V
.....	Vss-0.3V	Vdd+0.5V
.....	1.8V-5.5V	

6.2

(V_{DD} =5V =25)

I RC1	I RC1	OPTION 8MHz	-	8	-	MHz	
I RC2	I RC2	OPTION 910KHz	-	910	-	KHz	
I OH1	P63	I oh=4.4V	4.5	5	5.5	mA	
I OH2	P63	I oh=4.4V	5.5	6	6.5	mA	
I OH3	P63	I oh=4.4V	11	13	14	mA	
I OL1	I O P63	I ol=0.6V	10	11	12	mA	
I OL2	I O P63	I ol=0.6V	9	10	11	mA	
I OL3	I O P63	I ol=0.6V	21	22	23	mA	
I OL4	I O P63	I ol=0.6V	16	17	18	mA	
I OL5	P60, P61, P62	I ol=0.6V	26	27	28	mA	
I PH1	P63		80	100	130	μA	
I PH2	P63		80	120	130	μA	
I PD	P63	VDD	45	55	80	μA	
I sb1	1	VDD WDT	-	-	1	μA	
I sb2	2	VDD WDT	3	-	12	μA	
I op2	1 VDD=5V	I RC=8MHz 2clock	1.2	1.5	mA		
I op2	2 VDD=5V	I RC=910KHz 2clock	-	0.3	0.4	mA	
LVR		LVR	Vl vr-0.2	Vl vr	Vl vr+0.2	V	



6.3 AD

($V_{DD}=5V$ $V_{SS}=0V$ $T_a=25$)

V_{AREF}		$V_{AREF} - V_{ASS} = 1.5V$	1.5	-	V_{DD}	V
V_{ASS}			V_{SS}	-	V_{SS}	V
V_{AI}		-	V_{ASS}	-	V_{AREF}	V
IAI1	I_{VDD}	$V_{AREF}=V_{DD}=5V$ $V_{ASS}=0V$ $FS^{*1}=100KHZ$ $FIN^{*1}=1KHZ$ V_{REF} V_{DD}	-	1000	1400	μA
	I_{VREF}		-	-	10	μA
IAI2	I_{VDD}	$V_{AREF}=V_{DD}=5V$ $V_{ASS}=0V$ $FS^{*1}=100KHZ$ $FIN^{*1}=1KHZ$ V_{REF} V_{REF}	-	-	900	μA
	I_{VREF}		-	-	500	μA
RN		-	-	12	-	Bits
TAD	ADC	$V_{DD}=V_{AREF}=5V$ $V_{ASS}=0V$	1	-	-	μs
T_{SH}		$V_{DD}=3 \sim 5.5V$ $V_{ASS}=0V$ $T_a=25$	4	-	-	μs
		$V_{DD}=2.5 \sim 3V$ $V_{ASS}=0V$ $T_a=25$	16	-	-	μs
TCN	AD	$V_{DD}=2.5 \sim 5.5V$ $V_{ASS}=0V$	14	-	24	TAD
TADD1	AD" ADRUN"	TAD $V_{DD}=2.5 \sim 5.5V$ $V_{ASS}=0V$	0.5	-	-	TAD
PSRR		$V_{AREF}=2.5V$ $V_{ASS}=0V$ $V_{IN}^{*1}=0V$ $2.5V$ $FS^{*1}=25KHZ$			2	LSB



6.4 VREF

($V_{DD}=5V$ $V_{SS}=0V$ $T_a=-40 \sim 85$)

VDD		-	1.8	-	5.5	V
I_{VDD}	DC	No load	-	-	250	μA
VREF		1.5, 2V, 3V, 4V	-	± 1	1.75	%
Warm up Time		VDD=VDDmin-5.5V, Cl oad=19.2pF Rl oad=15.36K	-	38	50	μs
VDDmin		-	-	VREF+0.2	-	V



6.5

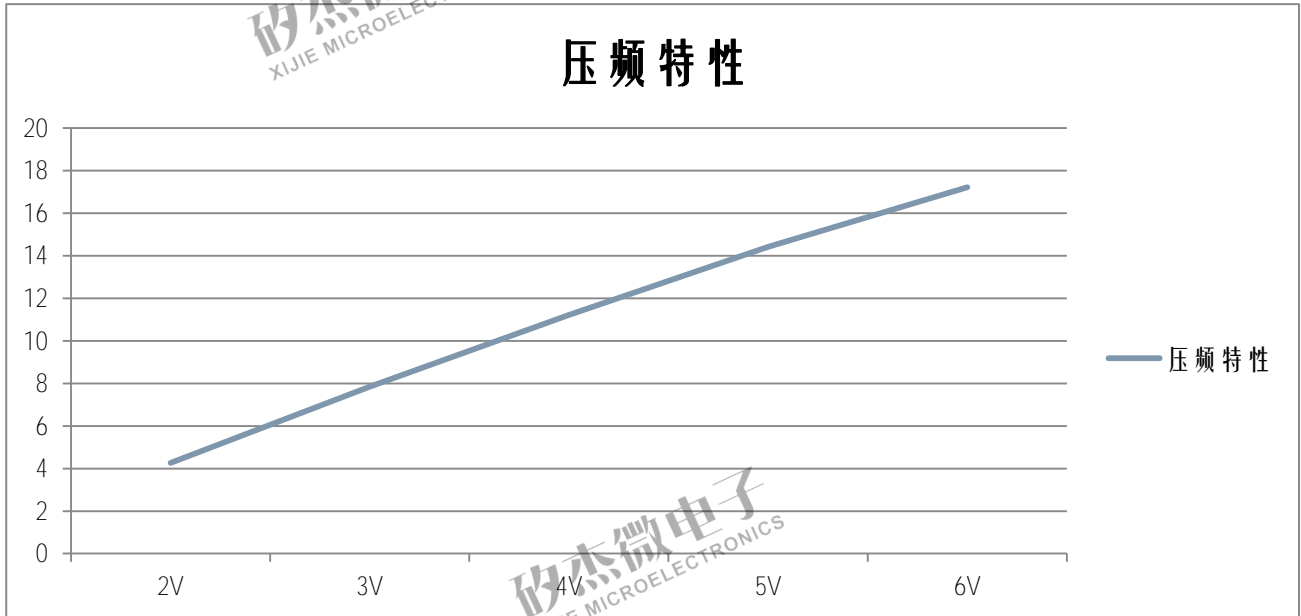
6.5.1

RC

-

25

(KHz)



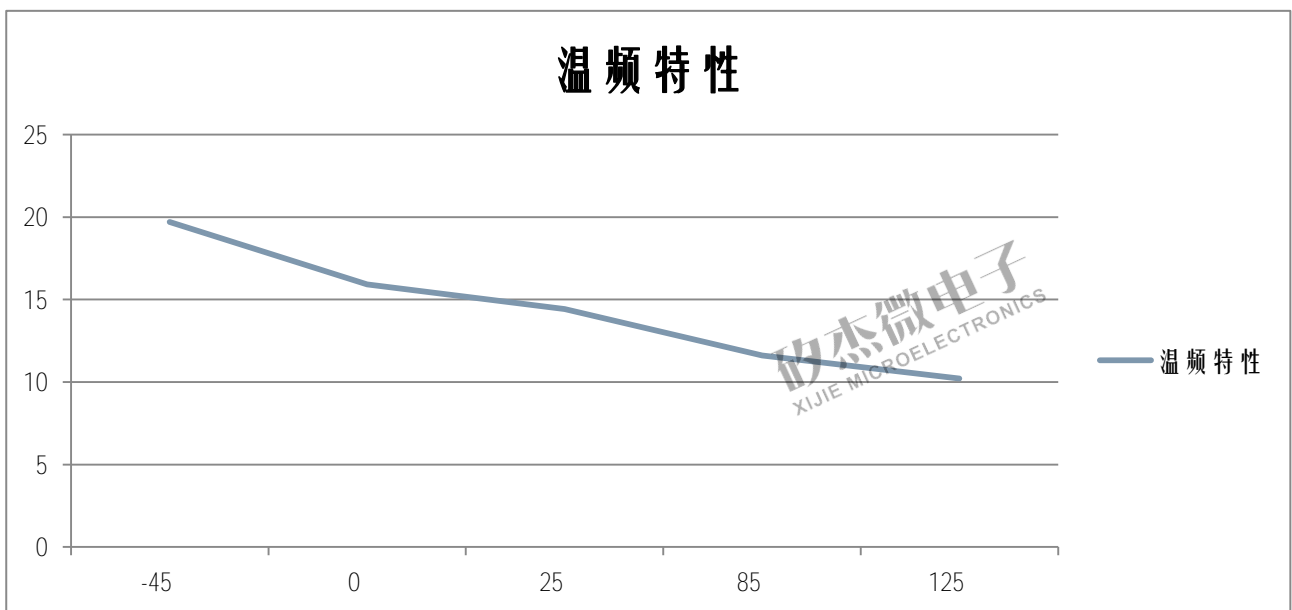
6.5.2

RC

-

5V

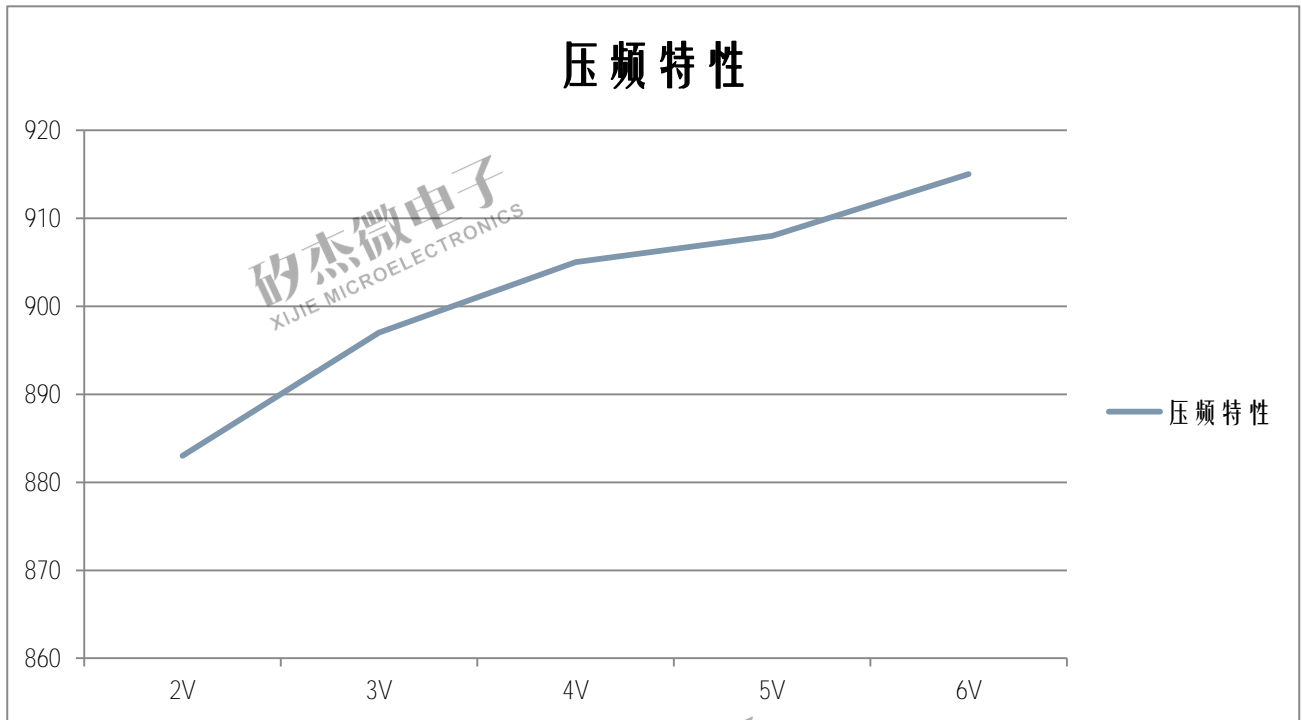
(KHz)





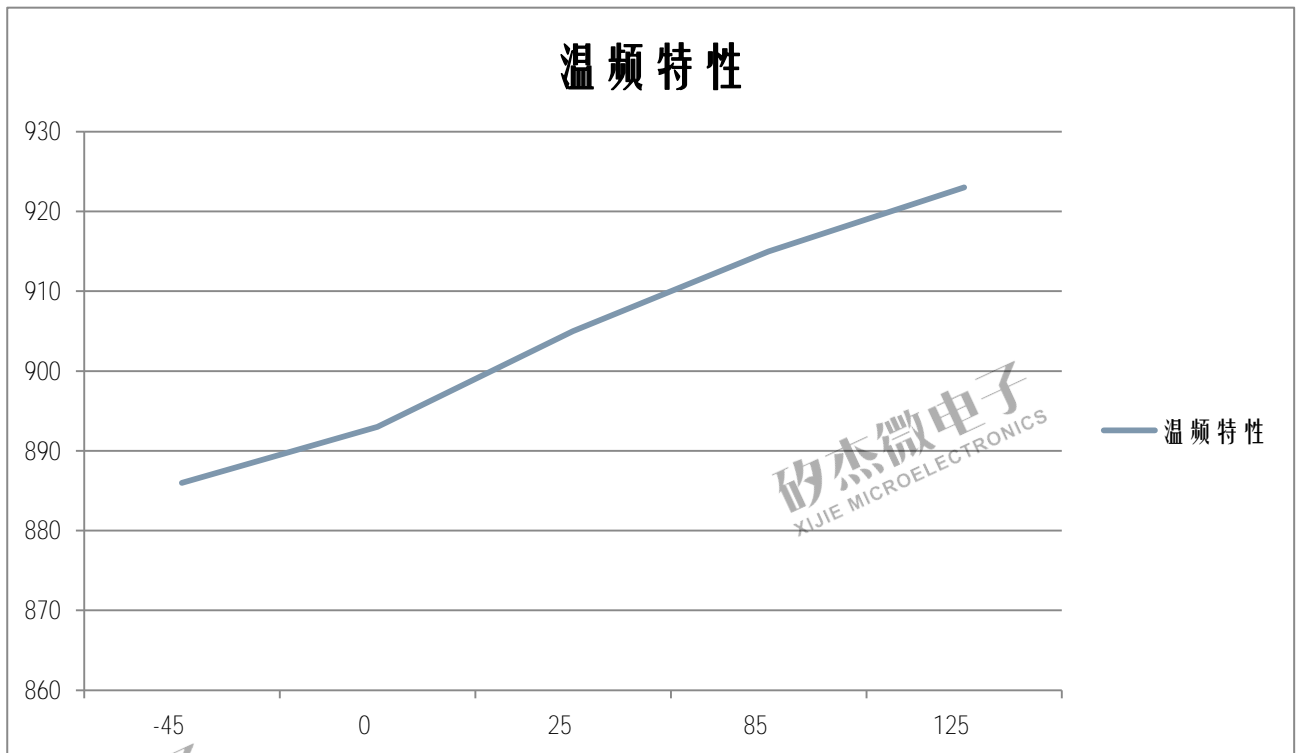
6.5.3 910KHz RC -

25 (MHz)



6.5.4 910KHz RC -

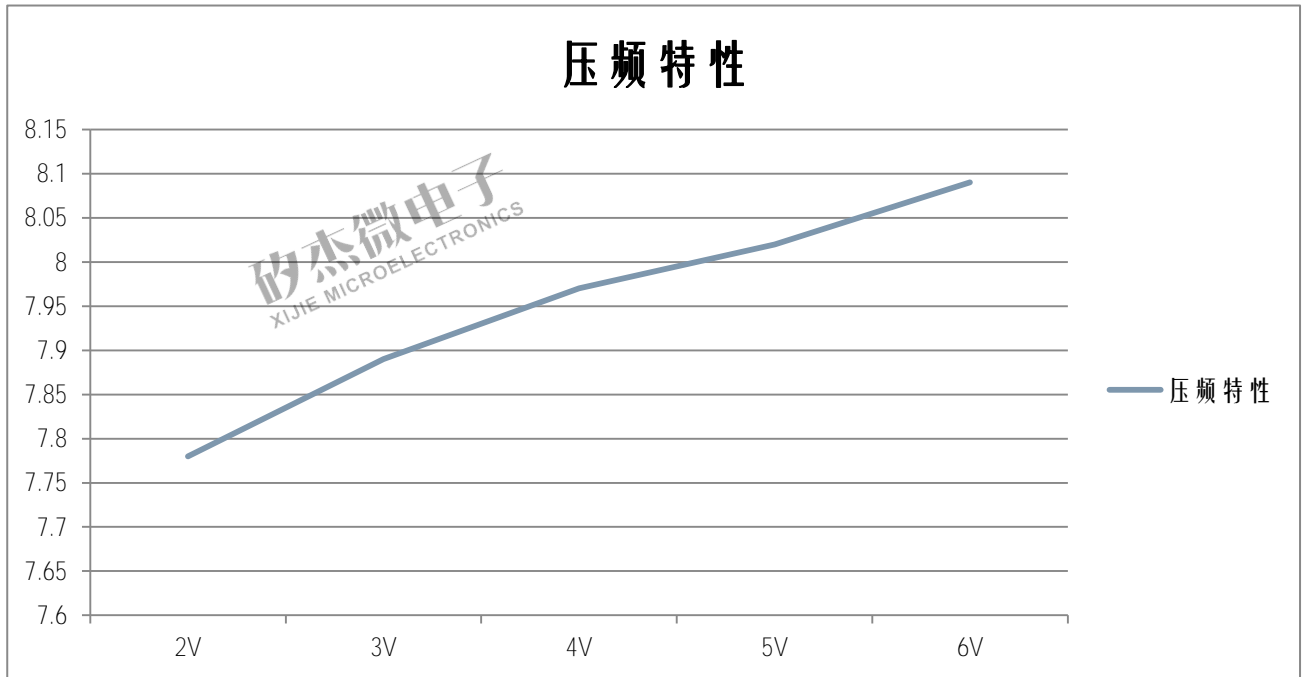
5V (MHz)





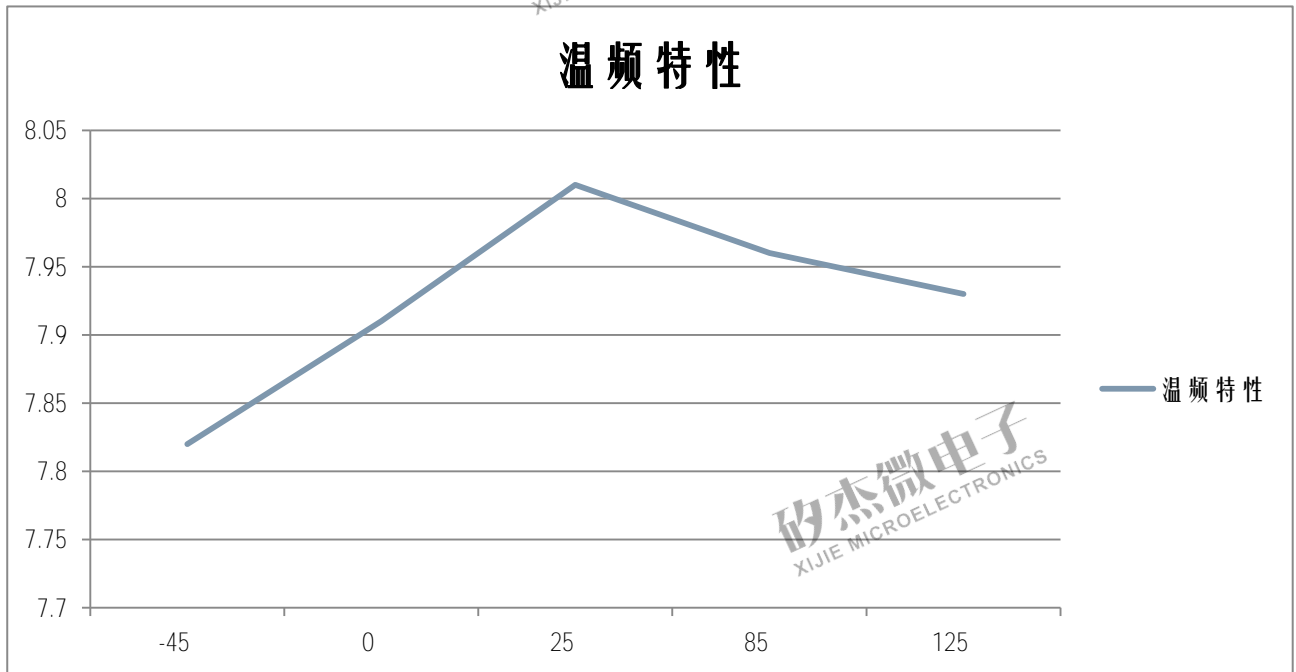
6.5.5 8MHz RC -

25 (MHz)



6.5.6 8MHz RC -

5V (MHz)

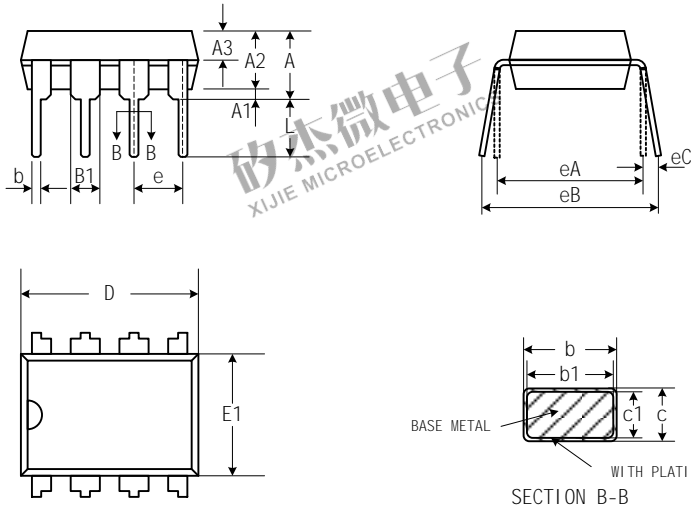




7.

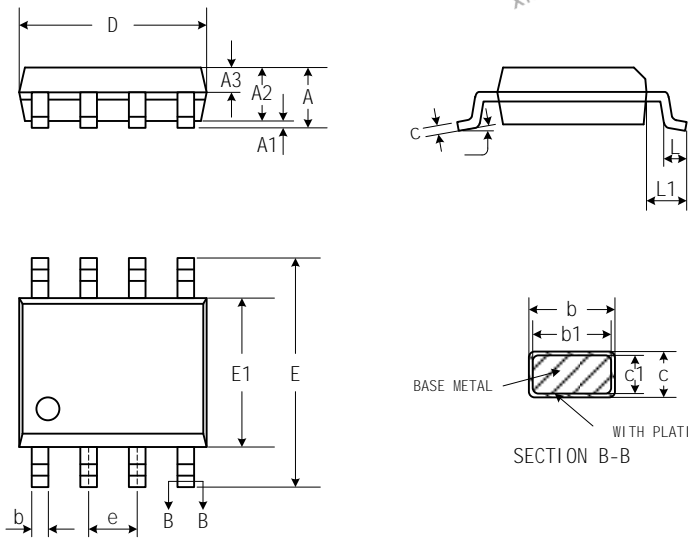
7.1 8PIN

DIP8



SYMBOL	MILLI METER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	-	-
A2	3.10	3.30	3.50
A3	1.50	1.60	1.70
b	0.44	-	0.53
b1	0.43	0.46	0.48
B1	1.52BSC		
c	0.25	-	0.31
c1	0.24	0.25	0.26
D	9.05	9.25	9.45
E1	6.15	6.35	6.55
e	2.54BSC		
eA	7.62BSC		
eB	7.62	-	9.50
eC	0	-	0.94
L	3.00	-	-

SOP8



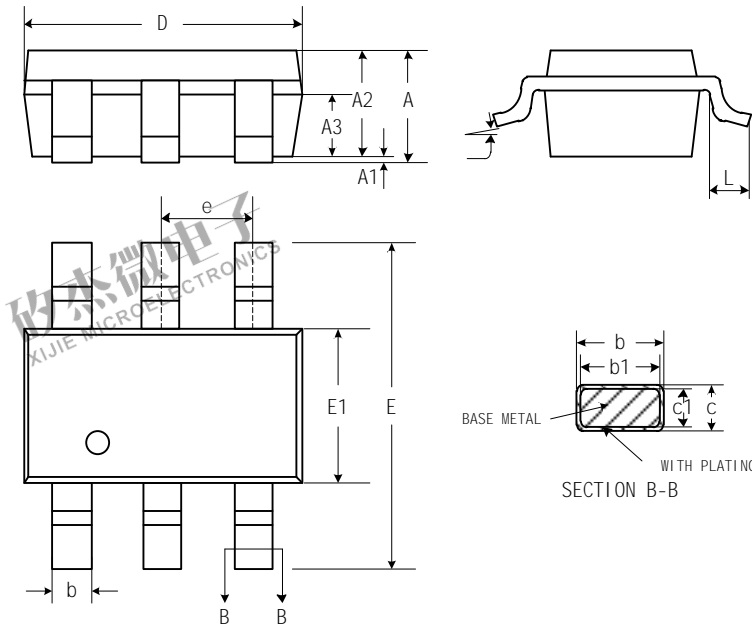
SYMBOL	MILLI METER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
	0	-	8°



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7.2 6PIN

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Symbol	mm			Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.35	—	—	0.053
A1	0.04	—	0.15	0.002	—	0.006
A2	1.00	1.10	1.20	0.039	0.043	0.047
A3	0.55	0.65	0.75	0.022	0.026	0.030
b	0.30	—	0.50	0.013	—	0.017
b1	0.30	0.40	0.45	0.013	0.016	0.018
c	0.08	—	0.22	0.006	—	0.008
c1	0.08	0.13	0.20	0.003	0.005	0.008
D	2.72	2.92	3.12	0.107	0.115	0.123
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.40	1.60	1.80	0.055	0.063	0.071
e	0.95BSC			0.037BSC		
L	0.30	—	0.60	0.012	—	0.024
	0	—	8°	0	—	8°

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